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ABSTRACT

The present invention relates to a stacked semiconductor chip package comprising a substrate, a first chip, a plate, and a second chip. The first chip is mounted on the substrate. The second chip comprises two opposed longitudinal sides defining a first length. The plate is mounted between the first chip and the second chip, and connects the first chip and the second chip. Corresponding to the two longitudinal sides of the second chip, the plate has two opposed longitudinal sides defining a second length. The second length is larger than the first length to expose the opposed longitudinal sides of the plate. An overflow adhesive portion is formed between the plate and the second chip, and the overflow adhesive portion exposes on the plate. Therefore, the testing instrument can detect the size of the overflow adhesive portion and the thickness of the adhesive layer so as to control the quality of the stacked semiconductor chip package. The adhesion strength between the second chip and the plate can be augmented to raise the reliability of the stacked semiconductor chip package product.